

END-USER APPS

AMD'S BULLDOZER: 32nm SOI

With performance, efficiency, and power optimization as top priorities, AMD's innovative Bulldozer architecture is built on 32nm SOI.

As of the Fall of 2011, AMD is shipping both client and server CPUs based on the new Bulldozer architecture. The first of the new APUs (CPU + GPU) incorporating Bulldozer modules will start shipping in 2012.

All of AMD's innovative new Bulldozer architectures are built on 32nm SOI technology fabbed by GlobalFoundries.

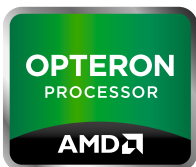
Bulldozer is the code name for AMD's next-generation CPU core, which targets the two key "heavy lifting" markets:

- > servers, and
- > the high-performance end of the client platform.

As indicated on the AMD roadmap, all of the company's CPUs for the "server" market – chips in the Opteron family – are based on the 32nm SOI Bulldozer architecture.

The roadmap for "client" products also shows key chip families for desktop processors and high-performance notebooks based on the 32nm SOI Bulldozer architecture.

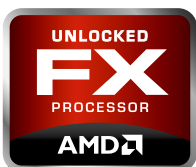
OPTERON/INTERLAGOS



Interlagos is the codename for AMD's 12- or 16-core 32nm SOI server processors based on the new "Bulldozer" processor core. It carries the AMD Opteron™ 6200 and 6100 Series processor brands and is supported by the AMD Opteron™ 6000 Series ("Maranello") platform.

Interlagos includes the world's first 16-core x86 processors. The first Interlagos shipments began in August 2011 to large custom supercomputer installations: 25,000 to Oak Ridge labs and 38,000 to Los Alamos, for example.

FX



The latest AMD FX series marks the first retail availability of Bulldozer-based processors. Available in 8-, 6- and 4-core configurations, these CPUs targets extreme multi-display gaming, mega-tasking and HD content creation for PC and digital enthusiasts.

The new FX includes the first-ever eight-core desktop processor, which took the Guinness World Record for the "Highest Frequency of a Computer Processor," hitting a top speed of 8.429 GHz.

UP NEXT: APUS

AMD has dubbed the company's new Fusion APUs the era of "Personal Supercomputing". The A-Series APUs, codenamed Llano, that started shipping in mid-2011 are based on 32nm SOI, but their CPUs are based on the previous generation of the x86 CPU architecture, and as such are not yet Bulldozer.

However, the next generation in the A-Series APUs, codenamed Trinity and scheduled for release in 2012, will also be based on 32nm SOI with next-generation Bulldozer CPU cores.

POWER-OPTIMIZED DESIGN

The Bulldozer architecture is based on "modules" of two cores each. AMD explains that this means two simultaneous threads can be executed more efficiently than two threads running on a single integer core.

For each two-core module, there is a shared 2MB L2 cache. The shared L3 cache varies from 8MB to 16MB, depending on the processor.

The Bulldozer design is new from the ground-up. It required co-development of power efficiency, timing, and functionality¹. The team reduced leakage power by 95% when both cores are idle by module-level VSS (rather than VDD) power gating, first used in the 32nm Llano CPU. SOI enables this to be done without extra processing steps².

The L1 caches use an 8T storage cell. The design team said that the change from a 6T cell in 45nm to 8T in 32nm improved the low-voltage margin and read timing and reduced power³.

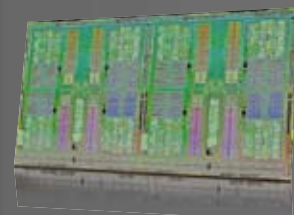
This game-changing architecture on SOI promises an exciting new era of high performance and low power in systems ranging from sleek but powerful notebooks to the fastest supercomputers on the planet. ●

Thank you to AMD for help on this article.

BULLDOZER SPECS

Bulldozer modules⁴:

- > each module has 2 cores
- > 213 million transistors/module
- > 11 metal layers, 32nm SOI, HKMG
- > 0.8 – 1.3V operation
- > Area/module: 30.9mm² (for a 2-core CPU module + 2MB L2 cache)



(Courtesy: AMD)

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1. Design Solutions for the Bulldozer 32nm SOI 2-Core Processor Module in an 8-Core CPU. Tim Fischer et al. IEEE ISSCC 2011, p.78.
 2. An x86-64 Core Implemented in 32nm SOI CMOS, by Ravit Jotwani, et al. IEEE ISSCC 2010, p. 106.
 3. Idem, Fisher et al.
 4. Idem, Fisher et al.

FD-SOI: 28nm AND BEYOND



By **Thomas SKOTNICKI**,
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STMicroelectronics
www.st.com

The multi-functional system-on-chips (SOC) needed at the heart of the next generations of wireless, high-performance, low-power multimedia devices have very different needs than the mono-functional processors of the past. Traditionally, the trade-off for computers and servers has been accepting high operational voltages (V_{dd}) and high stand-by leakage in return for high-performance. This is obviously not an acceptable trade-off for mobile internet devices.

In a mobile world, high-performance must go hand-in-hand with low-operation V_{dd} and low stand-by leakage. That requires different technologies. As we approach the 20/22nm node and beyond, traditional planar-bulk technologies cannot meet these requirements. The choice comes down to either a planar fully-depleted (FD) SOI solution or a FinFET solution. At STMicroelectronics, we call our flavor of planar FD-SOI UTBB, for ultra-thin body & box. As such, it leverages SOI wafers with both ultra-thin top silicon and ultra-thin buried oxide (BOX). Where more practical, we use a hybrid SOI/bulk configuration, wherein certain devices are placed in the bulk silicon that has been exposed by etching back the insulating BOX layer.

The results we've obtained make UTBB a compelling option.

Designing a good SOC involves using the right blend of low-, standard- and high-threshold-voltage (V_{th}) devices according to the target application and how it's being used at any given time. Our FD-SOI technology can handle multiple V_{th} devices and I/Os through a cost effective approach, solving challenges for low-power operation (LOP), low-standby power (LSTP) and analog and high-performance (HP) needs.

UTBB AT 28nm

ST's UTBB technology may be a good candidate even for the 28nm node, as it would provide a boost in speed before 20nm bulk technology is ready. Therefore, we have explored an industrial solution for its implementation.

Our objectives that we met for FD-SOI at the 28nm node were as follows:

STMicroelectronics sees its flavor of planar FD-SOI as an excellent response to the complex needs of mobile multimedia chips.

- > Demonstrate with respect to 28 LP Bulk :
 - + 30% Performance at same V_{dd} (1V)
 - or 40% lower power consumption for at least the same performance
- > Demonstrate feasibility of "easy" porting from Bulk to FD-SOI
- > Demonstrate manufacturability (including SRAM yield) of FD-SOI/UTBB (with 7nm top silicon thickness and 25nm buried oxide thickness)

With respect to porting the design, the goal of "easy" porting means:

- > the design only needs recharacterisation of critical paths
- > FD-SOI masks are redefined from Bulk by CAD2MASK.
- > Spice models are available for all devices

The process flow is derived from 28LP Bulk of the ISDA Alliance: Metal Gate First and no stressors. Out of 15 major process modules in the Front-End of Line, only 3 are specific to the FD-SOI process. The number of masks is similar to 28 LP Bulk (actually with a saving of 2 or 3, which could be used for analog adjustments in Hybrid bulk/SOI parts if needed).

More than 25 implant steps are saved vs. 28nm LP Bulk for two V_{th}s. This eliminates 15% of the process steps and results in a process cost saving of 10%. So as long as the SOI substrate cost overhead is less than 10% of the bulk process cost, the FD-SOI process is

more cost-effective than the bulk LP process.

It is worth noting that the relative impact of the substrate cost will be more favorable to FD-SOI at subsequent nodes, since the process becomes more complex on bulk and adds more metal levels.

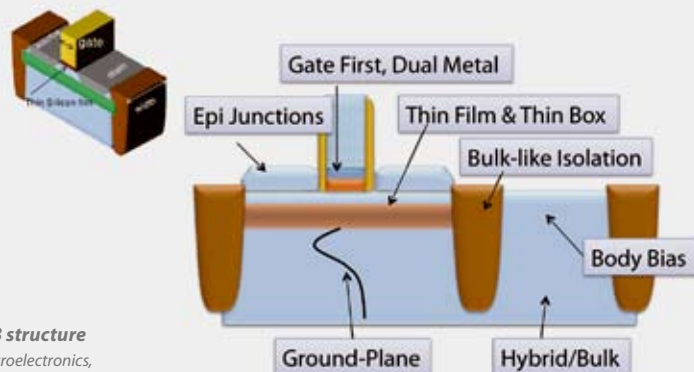
DIBL: THE SOC PERFORMANCE METRIC

The drive current, I_{on}, has long been the key metric for speed in high-performance microprocessors. But, especially for multimedia SOCs, the effective current I_{eff} is a much better metric and is heavily dependent on DIBL (Drain Induced Barrier Lowering). The lower DIBL of UTBB transistors reflects their superior electrostatic control and leads to higher performance. The influence of DIBL on maximum operating frequency is more pronounced for higher V_{th}s and/or lower V_{dd}, which explains why this parameter is crucial for low-power multimedia SOCs – which use higher V_{th}s than high-performance microprocessor chips.

V_{th} ADJUSTMENT AND PERFORMANCE RESULTS

The means to adjust V_{th} constitute a fundamental difference between bulk and FD-SOI devices.

On short devices in bulk, V_{th} is controlled primarily by channel doping. V_{th}s for logic



FD-SOI/UTBB structure
(Courtesy: STMicroelectronics,
IEEE SOI Conference 2011)

and SRAM can be adjusted independently.

In FD-SOI, however, V_{th} is controlled primarily by the gate stack on short and long devices in both logic and SRAM. By also playing upon channel length and ground plane implant below the BOX, we are able to obtain all the V_{th} s we need for our 28nm FD-SOI technology. According to its type (n or p), the ground plane (GP) can shift V_{th} up by more than 50mV (in the case of our 25nm BOX). GP implants also suppress the depletion depth below the BOX for better DIBL, and improve the effect of body biasing.

Body bias is a powerful performance booster usable at different V_{dd} points -- at low voltages, for example, speed is increased by 30%. The Ion/Ioff trade-off is not hurt (body-biasing simply shifts the operating point along the technology's Ion/Ioff curve), even for body bias voltages up to 2V. This flexibility is not available with FinFET, and while body bias is possible with planar bulk, at 28nm it is of limited practicality and effectiveness.

We then compared the 28nm FD-SOI to a 28nm bulk low-power-oriented 'LP' process and to different performance-oriented 'G'-type processes, on a DDR3 Memory Controller.

The results indicated FD-SOI had:

- > comparable performance to the "G"-type processes at high V_{dd} , with additional room for overdrive (and without the complexity of 'G'-type processes)
- > overall best performance across all practical V_{dd} values
- > a competitive advantage at low V_{dd} , with over 40% performance advantage over 'G' at 0.6V power supply
- > best power efficiency

Additional benchmarking on an ARM Cortex-A9 is confirming these results.

20nm GOALS

We want to propose a differentiated technology at 20nm node providing a 20% boost in performance versus 20LPM at the same V_{dd} . We also want it to be competitive versus a potential Trigate SOC at 22nm.

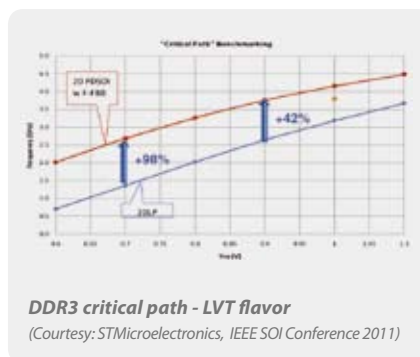
Under our 20nm UTBB FD-SOI scheme, performance will be boosted by dynamic control of a Full-Forward Body Bias (F-FBB) architecture. V_{th} modulation sources will include gate stack, ground-plane, counter-doping, body-bias and L poly-bias.

We have now compared our FD-SOI with bulk

and FinFETs at 20nm, with impressive results. While FinFETs and UTBB FD-SOI very much resemble one another (in fact, a UTBB device looks rather like a FinFET tipped on its side), with FD-SOI we are seeing:

- > a large gain in performance: 42% at 0.9V and 98% at 0.7V
- > best performance
- > G-like performance on an LP process
- > best power efficiency

Work by Leti and by IBM and partners also shows excellent SRAM transistor matching. UTBB was also found to have much lower threshold voltage variability, thanks in large part to the undoped channel. This in turn enables smaller SRAM cells and/or lower minimum voltages (V_{min}) – a gain of 150mV, which translates into significantly lower power consumption. We have determined that the SRAM remains fully functional as low as $V_{dd}=0.4V$.



14nm TO 8nm

An FD-SOI roadmap through 14nm indicates an orderly and logical progression. Leti has shown that further thinning of the insulating BOX layer enables FD-SOI scalability down to 8nm with top silicon thickness (TSi) no thinner than ~6-7nm (post-processing).

Soitec's Xtreme SOI wafers with ultra-thin BOX (25nm) is ramping to volume this year, targeting the 28nm node. With SEH and a third supplier on tap, the supply chain is in place.

STRAIGHTFORWARD MOVE TO 28nm

ST has been working on FD-SOI for over 10 years. We have research programs or partnerships on 3 sites : Crolles, Leti, and IBM Albany NanoTech. We have collaborated with Soitec for wafer supply.

The key technology elements for UTBB have been demonstrated.

The move from R&D to an industrial process of 28nm FD-SOI technology is for us (and for our partners) an efficient and straightforward response to the world-wide competition. The extension of FD-SOI towards the 20nm and 14nm nodes is also in preparation with new boosters to further increase the performance growth rate.

UTBB FD-SOI promises to give STMicroelectronics a significant edge in both the near term and for years to come. ●

UTBB SOI

C. Fournier-Benjamin et al., EDSS 2009 (ST-LETS)

L_g 35nm

Ti Ultra-thin

Box 10nm

FinFET

Yang, Sematech, Nov 2008

Topic	FD SOI	FinFET on Bulk
Performance metrics	Better	10% lower performance
Power metrics	Better	100mV higher supply Increased variability
Low power features	Ultra powerful Body Biasing Efficient multiple V_t	No Body Biasing Low efficiency Multiple V_t
Design Compatibility	Easy SOC migration from bulk	New technology implementation
Process Integration	Simple Process (Gate First, 20% FE steps to redevelop vs BULK)	Complex process

FinFET No room for Body contact

20nm FD-SOI vs FinFET: summary table
(Courtesy: STMicroelectronics, IEEE SOI Conference 2011)

INTERVIEW:

HOW NXP'S SOI TECHNOLOGY ENABLES MAJOR ADVANCES IN AUTOMOTIVE POSITION SENSORS

Guenter Reiniger, Marketing Manager for NXP's Automotive Sensors, explains how SOI helps eliminate the need for external components in a new magnetic sensor family.

Advanced Substrate News (ASN): NXP recently announced the KMA210, the first in a new family of magnetoresistive (MR) sensor chips. What is it used for?

Guenter Reiniger (GR): The KMA210 is a position sensor for automotive applications wherein a precise mechanical angle needs to be measured. So on one hand you can use it in things like electronic steering, active suspension and automatic headlight adjustment. But because it's very accurate and very robust, it's also an excellent choice for under-the-hood applications such as power train, throttle control and air control valve measurements. And since it operates in temperature ranges up to 160°C, it's ideal for things like emissions control and clean diesel applications.

ASN: The MR technology isn't new – what's new about this chip?

GR: MR technology was pioneered by Philips and a few others over 30 years ago, so it's proven and robust. We've been selling MR sensors in very high volumes for many years – Continental alone has used over half a billion in its ABS systems. What's new

here is our ability to incorporate the signal-conditioning ASIC with the MR sensor in a full system-in-package solution. That's where the SOI comes in.

ASN: Why did you need SOI?

GR: Our customers now have to meet extremely rigorous requirements, especially with respect to safety, emissions controls, electromagnetic compatibility (EMC) and electrostatic discharge (ESD). Previous solutions involved the sensor plus separate bulk-silicon-based components that our customers would incorporate on a board. To cost-effectively incorporate the sensor with the requisite electronics in a single package, we need to put the signal-conditioning ASIC on 140nm SOI using our latest ABCD9 process technology.

ASN: Why is that?

GR: SOI gives our chip designers a number of advantages, such as:

- **Reduced resistance** for the transistor in the on-state (Rds(on)), so much less waste heat is produced, which we leveraged to make a much smaller chip.

- **Much greater packing densities**
- **Latch-up-free behavior**, since there are no parasitic junctions between N-type and P-type devices.
- **Ability to handle voltage spikes** from the starter motor or alternator
- **Greatly improved heat tolerance.**
- **Easy integration** of multiple power devices, bridge rectifiers, and flyback diodes on the same piece of silicon. In combination with a significant reduction in parasitic capacitance, this simplifies and speeds the chip design process.

ASN: In addition to the cost effectiveness for you, what advantages does SOI confer to your customer, the automotive designer?

GR: We created this product in very close partnership with our customers. By implementing the ASIC on ABCD9 SOI, the interface areas of the ASIC have 16V overvoltage protection – in bulk the chip would have been too big and too expensive. From the automotive designer's perspective, they can use the same socket they used for previous generations when it was just the sensor – but now they don't have to design a board to go with it – everything's in there. The device contains two embedded block capacitors (for Vdd and output) within the same package. And of course you get the advantages you always get with SOI: robustness in terms of EMC, ESD and high temperatures. The package really reduces system cost: there's no additional design, no boards, no external filter components, no lead frames. All told, the KMA210 position sensor with the integrated ASIC on SOI gives the automotive designer the key to a cheaper, smaller and more robust measurement solution.

ASN: What does the future hold?

GR: With ABCD9 on SOI, we are working on a next generation of these chips for temperatures up to 200°C. For next year, we'll also have a redundant version (with two devices in one package), and a version with digital output. While perhaps we could have done all this without ABCD9 and SOI, we couldn't have done it under the same commercial conditions. These are really cost-effective devices. ●

An example of how NXP's KMA210 magneto-resistive sensor would be used in a throttle position application. Because the KMA210 is manufactured using NXP's ABCD9 process technology on SOI, the signal-conditioning ASIC and the sensor are fully integrated in a system-in-package solution that requires no additional external components. (Courtesy: NXP)



ALL YOU NEED IS FD-SOI



By **Jean-Luc PELLOIE**,
ARM Fellow,
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ARM
www.arm.com

Bulk logic designs can be ported directly to FD-SOI for high-performing, low-power mobile apps.

Fully-depleted (FD)-SOI is a potential alternative to 20nm bulk. But what sort of the impact will that have on the design flow? The short answer is: very little.

Designs for low-power mobile applications in 28nm bulk benefit significantly in terms of increased performance and decreased power when ported to 20/22nm fully-depleted (FD)-SOI. From the designer's perspective, the port is essentially direct – really no different from any standard port to a smaller geometry.

Interconnects, routing and RC parasitics are identical. Logic, memories, low- and high-voltage I/O and analog parts are handled in the same way as on bulk. Where there are differences, they are more at the device/process level, and do not pose any particular challenges to the designer at this point. This includes SPICE models, antenna effect, ESD protection, I/O and analog, and back-gate bias.

20NM FD-SOI V. 28NM BULK

To get some clear figures on power and performance, ARM recently ported a Cortex-M0 from 28nm bulk to 20nm FD-SOI. We used the Cortex M0 implementation flow that was proven in 22nm SOI. This included:

- > synthesis, place and route, and the same reduced set of standard cells for 20nm FD-SOI and 28nm bulk
- > parasitics extraction for interconnects from the routed 22nm SOI M0 core (22nm SOI Back-End Of Line (BEOL) is considered to be the most representative of current bulk/FD-SOI 20nm BEOL)

	Synopsys	Cadence	Magma
Synthesis	Design Compiler	RTL Compiler	Talus Design
Place & route	IC Compiler	SoCE Nanoroute	Talus
Timing analysis	PrimeTime (NLDM, CCS)	ETS (NLDM, ECSM)	Talus (NLDM, CCS)
Power analysis	PTPX, PrimeRail (NLDM, CCS)	EPS, VoltageStorm	Talus
Signal integrity	PTSI	CeltIC	Talus
DFT	Tetramax		
Verification	Formality	Conformal	

ARM uses standard packages from the leading EDA vendors in SOI ASIC design.

- > characterization of 20nm FD-SOI and 28nm bulk standard cells (typical process corner and room temperature)
- > different voltages to create the corresponding .lib files that would be used for timing and power analysis of the M0 core: 0.7, 0.8, 0.9 and 1V
- > timings and power were compared for the routed M0 core based on 20nm FD-SOI and 28nm bulk characterizations (.lib).

In any next-node port, you typically expect to get a 25% improvement in performance, but in porting from 28nm bulk to 20nm FD-SOI, FD-SOI boosted the improvement far beyond the expected 25%. At a V_{dd} (supply voltage) of 1.0V, we saw a 40% improvement in performance. At 0.9V, we saw 66%. For V_{dd} of 0.8, we saw an 80% improvement. And for V_{dd} of 0.7, we saw an improvement of 125%.

Power is consistently reduced by 30%, and leakage holds steady.

Remember, this is a straight port, which gives us a baseline figure. There are several powerful process and design optimization techniques that can boost those numbers even higher without significantly increasing the complication factor.

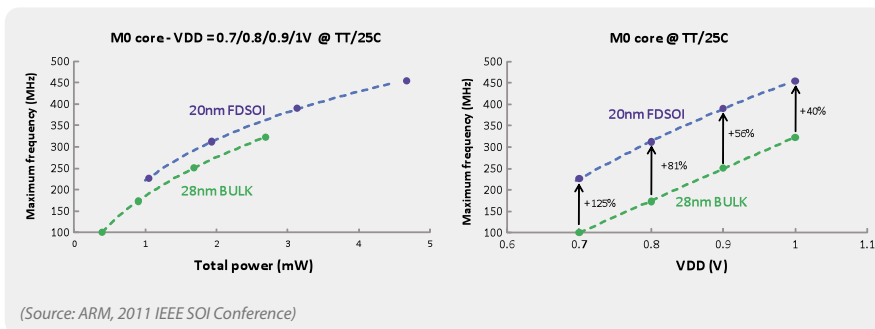
EXISTING DESIGN, TREMENDOUS RESULTS

The conclusions we have drawn are that:

- > a standard bulk ASIC design flow can be used for FD-SOI – don't expect any change
- > an existing bulk logic design can be directly ported to FD-SOI
- > you just need to check the timing closure – there is no timing variability (this is not PD-SOI)

FD-SOI should give tremendous advantages in terms of both power and performance. These low-voltage, high-performance chips are perfect for low-power applications, with the undoped channel in the low voltage SRAM resulting in higher margins. For some applications, RF features will also be improved if designers choose high-resistivity substrates.

FD-SOI is all a designer needs for high-performing, low-power mobile applications. And happily from the designer's point of view, FD-SOI is as simple as designing in bulk. ●



This article was adapted from "FD-SOI Design Portability from BULK at 20nm Node", which was presented at the 2011 IEEE SOI Conference.

FD-SOI PROCESSES ARE COST COMPETITIVE WITH BULK



By **Scotten W. JONES**,
President,
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A new study compares processes for the 20/22nm generation at a typical foundry.

Silicon On Insulator (SOI) has been in use for state-of-the-art integrated circuit (IC) manufacturing since IBM first championed the technology in the mid-nineties. SOI offers process technologists the option of reducing power or improving performance for a given process node.

As process technology has continued to advance it has become practical to manufacture SOI wafers with silicon layers that are thin enough for Fully Depleted SOI (FD-SOI). Also referred to as Extremely Thin SOI (ETSOI), FD-SOI processes offer process technologists the opportunity to significantly simplify the process of manufacturing an IC.

IC Knowledge, the world leader in IC cost and economics was retained by Soitec, the world leader in SOI wafer manufacturing, to compare the cost of a FD-SOI process versus a Bulk process for 22nm/20nm foundry logic processes.

THRESHOLD VOLTAGES

One of the challenges of state-of-the-art foundry processes is providing the multiple threshold voltages required for power management and performance. At a minimum an additional threshold voltage requires two threshold adjust masks and associated implants.

As process geometries have shrunk additional threshold voltages may also require tailoring of source/drain (S/D) extension and halo implants and even S/D contact implants (both extension/halo and contacts each require multiple implants to fabricate).

The result is a single threshold voltage can require up to five masks and fifteen implants.

FD-SOI on the other hand can provide multiple threshold voltages by alternative means (including the option to shift the threshold voltage by actively controlling the

biasing of the back gate), eliminating the need for threshold adjust masks and implants entirely.

PROCESS SIMPLIFICATION

An FD-SOI foundry process with eight metal levels and three threshold voltages can be fabricated with up to fifteen less masking steps and forty-eight fewer implants than a similar bulk process. The resulting process simplification was found to more than offset the higher cost of the starting SOI substrate and result in a cost competitive process versus bulk with better performance.

As processes scale down to 22nm/20nm and beyond standard bulk process transistors can no longer be scaled down without exhibiting unacceptable leakage properties. Techniques such as FD-SOI offer better control of the transistor channel and far lower leakage making them a viable technical solution to leakage problems. As has been shown in this study FD-SOI also offers an economically viable solution.

In conclusion FD-SOI processes offer sufficient process simplification to offset the additional cost of the starting SOI substrate and be cost competitive with bulk processes. ●

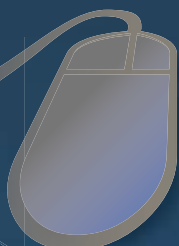
Note: the full FD-SOI cost report is available as a free download from IC Knowledge.

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PEOPLE

MOVERS AND SHAKERS



The leading producer of SOI wafers, Soitec was named NXP's Best Supplier for Front End Materials & Equipment. NXP was one of the first in the industry to use SOI. The relationship with Soitec dates back to 1995, when

the two companies began work together on the development of the (then Philips') breakthrough SOI-based ABCD technology. ●



Soitec also announced that Dr. Justin Wang has joined the company as senior vice president, corporate marketing and strategy. He is an industry veteran with over 15 years of experience in both the electronics and solar markets at TSMC. ●

TOP HONORS

The IEEE is once again giving two of its most prestigious awards to some of the SOI and advanced substrate industry's leading figures.

There are few greater honors in engineering than the IEEE Technical Field Awards (TFAs). And once again, people who work in advanced substrates are among the recipients of two major awards: the IEEE Andrew S. Grove Award and the IEEE Daniel E. Noble Award for Emerging Technologies.

The TFAs are awarded for contributions or leadership in specific fields of interest of



the IEEE. The prize items for these awards consist of a bronze medal, certificate, and honorarium. They are typically announced each summer. ●

THE GROVE AWARD

The IEEE Andrew S. Grove Award honors its namesake's lifetime achievements. It is sponsored by the IEEE Electron Devices Society, and presented to an individual for outstanding contributions to solid-state devices and technology.

The co-recipients of the 2011 IEEE Andrew S. Grove Award are **Judy Hoyt** and **Eugene Fitzgerald**. Professor Hoyt is with the MIT Department of Materials Science. Eugene Fitzgerald is the Merton C. Flemings-SMA Professor of Materials Science and Engineering and head of The Fitzgerald Group at MIT.

Hoyt and Fitzgerald are cited for "seminal contributions to the demonstration of Si/Ge lattice mismatch strain engineering for enhanced carrier transport properties in MOSFET devices." Their work on "strained" silicon and its application to SOI wafers is well-known in the advanced substrates community. (Professor Fitzgerald wrote about this work in ASN5, Summer 2006.)

The 2011 Grove Award will be presented at the 2011 IEEE International Electron Devices Meeting (IEDM), which takes place in December 2011 in Washington D.C., USA.

The IEEE has also announced that the 2012 Grove Award will feature another SOI luminary: Jean-Pierre Colinge, Head of the Microelectronics Centre, Tyndall National Institute, University College Cork, Cork, Ireland. The award recognizes Dr. Colinge "for contributions to silicon-on-insulator devices and technology." He is heralded in the industry for his seminal and continued work in multigate FETs that paved the way for FinFET and TriGate architectures. The actual ceremony will take place at the end of 2012. Dr. Colinge and his work have been featured in many editions of ASN.

Previous Grove winners with strong ties to the advanced substrate community include Bijan Davari (IBM, 2010) and Dimitri A. Antoniadis (IBM, 2002). ●

THE NOBLE AWARD

The IEEE Daniel E. Noble Award for Emerging Technologies honors Dr. Daniel E. Noble, Executive Vice Chairman of the Board emeritus of Motorola. It is given for outstanding contributions to emerging technologies recognized within recent years.

The 2011 Noble Award was given to **Mark L. Burgener** and **Ronald E. Reedy** for "basic research and development of silicon on sapphire technology culminating in high-yield, commercially viable integrated circuits". Dr. Burgener is vice president of advanced research and Dr. Reedy is the chief operating officer at Peregrine Semiconductor Corporation, San Diego, California.

In particular, the award recognizes their persistence and contributions in making silicon-on-sapphire (SOS) commercially viable for producing integrated circuits with

improved speed, lower power consumption and more isolation compared to bulk silicon circuits.

The ceremony for the 2011 Noble Award took place during the IEEE/MTT-S International Microwave Symposium (MTT 2011) in June 2011 in Baltimore, MD, USA.

The IEEE also announced the recipient of the 2012 Noble Award: Subramanian S. Iyer, for "the development and implementation of embedded DRAM technologies." Dr. Iyer is Distinguished Engineer & Chief Technologist, Semiconductor Research & Development Center, IBM Systems & Technology Group. He wrote about the role of SOI in "eDRAM" technology in ASN6 (December 2006). The technology is now at the heart of IBM's latest offerings. ●



DRIVING ROADMAPS

Highlights from the IEEE 2011 SOI Conference include presentations by ST, ARM, IBM, Intel, Leti, Peregrine, GlobalFoundries and more.

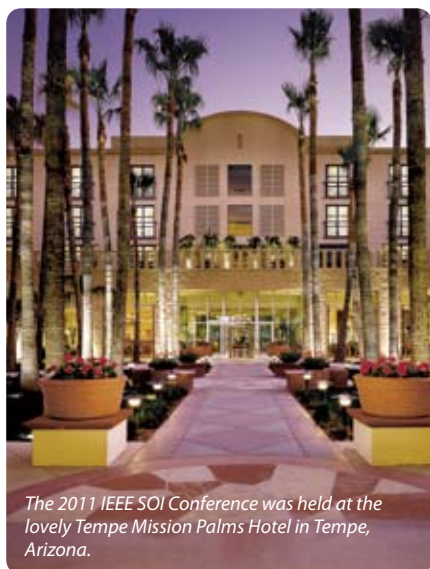
The 2011 IEEE SOI Conference, held in Tempe, AZ this past October was not one to miss. Highlights include excellent and insightful papers from ST, ARM, IBM, Intel, Leti, Peregrine and GlobalFoundries, plus many more that indicate SOI-based technologies are at the heart of many a roadmap.

Consider some of the plenary talks.

First was *Competitive SOC on UTBB SOI* by Thomas Skotnicki of ST Microelectronics. This was a detailed presentation on ST's vision for planar fully depleted (FD) SOI (which he described as equivalent to a FinFET rotated by 90 degrees). Here are some of the key points:

- > ST's FD objectives are +30% performance at Vdd 1V and +40% at Vdd - 0.1
- > The FD Process saves 10% cost over the equivalent bulk process, mainly because there are 25 fewer implantation steps.
- > The process options for 28, 20, and 14nm were detailed.

Next up was *FD-SOI Design Portability from BULK at 20nm Node* by Jean Luc Pelloie of ARM. Jean Luc, who is ARM's Director of SOI Technology, described how a Cortex M0 implementation flow was proven in 22nm SOI. He emphasized that the design migration to FD-SOI is straightforward



The 2011 IEEE SOI Conference was held at the lovely Tempe Mission Palms Hotel in Tempe, Arizona.



Jean Luc Pelloie, Director of SOI Technology, ARM, presenting at the 2011 IEEE SOI Conference.

in terms of EDA flow: the interconnects routing, parasitics are identical, and FD-SOI transistors' electrical behavior is similar to bulk transistors.

There's no floating-body effect, no history effect, no timing variability, he reminded attendees. Logic and memories are identical. That said, further optimization can be done to account for different electrical features at the device level. The few differences specific to FD-SOI are not design-related but more process/device-related (SPICE models, antenna effect, ESD protection, potential parasitic bipolar, and back-gate bias).

Consider the improvements in performance that ARM's seeing on an M0 core on 20nm FD-SOI vs. 28nm bulk: 40% better at 1V, 56% at 0.9V, 81% at 0.8, and an amazing 125% better performance at 0.7V.

As SOI Consortium Director Horacio Mendez pointed out in ASN this summer, you typically expect to get about a 25% improvement in performance moving to the next node. But ARM's showing that if you move to the next node and move to FD-SOI, you get really phenomenal results, especially at the lower supply voltages.

In the Hot Topics Session, Bruce Doris (IBM) announced new High Performance values for FD-SOI in his presentation on *The Future of SOI Transistor Technology*:

- > At Vdd 1V, for Ioff 100nA, he reported NFET Ieff 0.82 and Isat 1.4 mA/ μ m

- > At Vdd 1V, for Ioff 100nA, he reported PFET Ieff 0.68 and Isat 1.2 mA/ μ m

Integration of photonics and electronic circuits on SOI was the subject of both Yuri Vlasov's (IBM) plenary talk, and Juthika Basak's (Intel) Short Course.

A half-dozen excellent presentations by Leti during the short course and invited papers explored FD-SOI from many perspectives, including scaling paths, properties and challenges/solutions.

Papers from Peregrine and Soitec showed some impressive results for their new mass-produced bonded silicon-on-sapphire (BSOS) wafers for RF applications. In *Strain Reduction in Silicon-on-Sapphire by Wafer Bonding* BSOS films showed 56% higher electron mobility than traditional SOS; and RF switch performance in BSOS was better than GaAs PHEMTs.

J.P. Raskin (UCL), who's doing some fascinating work, presented *Sensing and MEMS Devices in Thin Film SOI MOS Technology*.

And finally, a team from MIT/Lincoln Labs once again slipped in a tantalizing concept in their late paper submission entitled *SOI Circuits Powered by Embedded Solar Cell*.

The online version of ASN will be covering more of the papers presented at this conference in upcoming PaperLinks articles. But clearly, the 2011 IEEE SOI conference was an excellent one. ●

SOI BONDING AT 450mm



By **Thomas GLINSNER**,
Head of Product Management
EV Group
www.evgroup.com

EVG's new wafer bonding system is a fully automated tool for production-level fabrication of 450mm SOI wafers.

Transitioning to larger wafers heightens the need for process uniformity. Wafer bonding is no exception, as process parameters must be applied with a high degree of both precision and uniformity. This requirement will become particularly critical within the next couple of years, as adoption of silicon-on-insulator (SOI) substrates will intensify in tandem with the impending shift to 450 mm wafers. Wafer bonding is a crucial technique for SOI wafer fabrication, as it enables formation of high-quality, single-crystal silicon films on an insulating layer: the essence of an SOI substrate.

To ensure chipmakers' access to these highly stringent wafer bonding capabilities, EV Group recently announced the semiconductor industry's first bonding system for the fabrication of 450 mm SOI wafers. Dubbed the EVG850SOI/450 mm, the new system will support and facilitate the industry transition to 450 mm wafers from the current 300 mm standard. Leading SOI wafer provider Soitec will qualify and develop

processes on the EVG850SOI/450mm after its installation in spring, 2012.

SOI is expected to play an enabling role in the migration to 450 mm, because it not only addresses most of the associated scaling challenges, but it also delivers better power/performance for sub-22-nm CMOS and 3D IC technologies compared to similar-geometry bulk CMOS.

FULLY AUTOMATED PRODUCTION TOOL

The new EVG850SOI/450 mm wafer bonding system leverages EVG's strengths in wafer bonding technology – and SOI bonding, specifically – to create a fully automated tool for production-level fabrication of SOI wafers. It consists of two process modules: a cleaning module for cleaning and pre-conditioning of wafers before wafer bonding, and an SOI pre-bonding module. In the pre-bonding module, the two silicon wafers are joined together either in a vacuum or in an

atmospheric chamber. The tool is equipped with state-of-the-art 450 mm load ports and front opening unified pods (FOUPs).

The first tool in EVG's 450 mm arsenal, the new bonder will serve as the key starting point for the production of 450 mm SOI wafers, and can be utilized for the development of other EV Group 450 mm products, such as mask aligners and coating systems. An extension of the system with additional modules is planned as a further step to increase wafer throughput.

As most of the required metrology tools are not ready for 450 mm wafers yet, the system will allow for processing of 300 mm and 450 mm wafers and parts of the evaluation program can be performed on 300 mm wafers. While one size doesn't fit all, the new EVG wafer-bonding system can fit 300 mm and 450 mm of advanced SOI wafers, helping ensure a smooth transition to the 450 mm generation. ●



The new EVG850SOI/450 mm wafer bonding system.



Charting the Way for Porting SOCs to FD-SOI



By **Horacio Mendez**,
Executive Director,
SOI Industry Consortium,
www.soiconsortium.org

Members of the SOI Consortium have released a major white paper addressing the porting of SOC designs from bulk to FD-SOI.

SOC designers face a critical juncture at 20/22nm. Choices must be made whether to stay on bulk CMOS, change to a FinFET architecture, or move to planar, fully-depleted (FD) SOI-based CMOS.

Power management and variability control are making scaling in bulk CMOS much more complex. The FinFET option, on the other hand (which can be on bulk or SOI) raises significant development and manufacturing challenges in the short term (although these will probably be less of an issue as time goes on). The planar FD-SOI option, however, is very attractive both for the short and longer terms with respect to cost, performance, power and complexity, especially for low-power, high-performance challenges.

FD-SOI has been shown to enable major savings in power (40%) and/or a significant increase in performance (25 to 80% – depending on the V_{dd} and design type) over low-power bulk technology. A recent study by IC Knowledge found that FD-SOI will be more cost-effective than standard bulk CMOS largely thanks to the fact that it requires significantly fewer processing steps.

However, the SOC designer may well ask how FD-SOI would impact the design flow.

Member companies of the SOI Consortium – including ARM, Leti, UCL, IBM, GlobalFoundries and Soitec – have now addressed the concerns of designers by issuing a major technical white paper entitled, “Considerations for Bulk CMOS to FD-SOI Design Porting”.

It is available immediately as a free download from the SOI Consortium website.

SCOPE OF THE PAPER

The scope of the study is to examine the efforts required to port existing bulk CMOS designs to FD-SOI at the same node. It considers both bulk-to-FD-SOI IP Porting and full chip design porting.

With respect to the full chip design porting, it considers two potential paths:

- > the straightest possible porting from bulk to FD-SOI – ideally, no change in place-and-route, and as close as possible to keeping the same GDS with all FD-SOI-specific updates automatically handled at mask generation;
- > or, optimizing the SOC implementation to take full advantage of FD-SOI options like back-biasing.

A section on FD-SOI design specificities considers in significant detail devices and electrical characteristics that are addressed at the technology level. It also examines any impacts at the designer level, and indicates what is foundry-dependent.

The heart of the document is a section called “Impact Per Design Domain”. This addresses the impact of an FD-SOI port on logic library cells, memory compilers, I/Os and ESD protections, analog & mixed-signal IP, and the choice of porting approach (fastest vs. most optimized) all the way down to sign-off considerations.

For designers considering the “most optimized” approach, the appendices go into great detail on back-biasing for VT shifting or tuning (which is more efficient than, although similar to the body-biasing used in some bulk designs), as well as “native” multi-VT.

Finally, the References section is an excellent resource, listing the most important FD-SOI papers presented at major conferences over the past few years – including VLSI, IEDM, ISSCC, the SOI Conference and more.

The goal of this white paper is to really address the issues at a technical level. However, it should also be useful to executive decision makers. We welcome your feedback. You will also find that there are dozens of technical presentations available on the SOI Consortium website addressing specific topics. Please feel free to contact the Consortium for more information or if you’d like to engage in more in-depth discussions regarding the upcoming choices we all face. ●

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Considerations for Bulk CMOS to FD-SOI Design Porting – Key Excerpts



The latest white paper from SOI Consortium members is loaded with technical information. The full paper is available on the website. Here are some of the highlights.

In approaching a bulk-to-FD-SOI port, different perspectives can be taken:

- **IP Porting:** The focus may be to easily port the libraries and other IP available in Bulk to FD-SOI, accepting some redesign work at System-On-Chip (SOC) integration level.
- **Full chip design porting:** Alternatively, it may be important to assess the efforts needed to start from an existing SOC design on Bulk and port this full chip to FD-SOI.

KEY MESSAGES

The efforts required to port a design will depend on the exact foundry offering and associated Design Kit. Nevertheless, in essence:

- Designing for planar FD-SOI technology is the same as designing for planar bulk CMOS.
- IP Porting from Bulk to FD-SOI (same node, same foundry) can be very direct, for worthwhile benefits at fast time-to-market – with some more work for Analog IP.
- Further optimization efforts can bring even greater product differentiation.
- SOC Porting from Bulk to FD-SOI can be very direct – and appropriate technology choices by the foundry (for example VT offering) shall facilitate this.
- FD-SOI offers efficient knobs to further optimize SOC performance.

CIRCUIT-LEVEL BENEFITS

FD-SOI transistors, because of their ultra-thin body, have a much closer-to-ideal behavior than classical planar bulk CMOS. For designers this translates to unique advantages at the circuit level, including:

- **Faster operation** at equivalent leakage, with the relative performance gap growing tremendously in the low V_{dd} range,
- Or, conversely, the ability to reach **the same target frequency at significantly lower V_{dd}**, enabling large power savings,
- Drastically reduced **variability**, with a positive impact on V_{DDmin} of SRAM arrays, **chip-level leakage**, etc.
- **Enhanced efficiency of low-power design techniques** such as DVFS (Dynamic Voltage and Frequency Scaling), back-bias, etc.

STANDARD CELLS

Direct porting is an option for seeing worthwhile benefits with the fastest time-to-

market. It involves swapping bulk transistors for FD-SOI transistors at constant cell layout and re-characterizing the cells.

Alternatively, if ultimate performance is sought, re-optimization of selected cells vs. exact transistor characteristics may further improve the results. The exact return on efforts would be confirmed by checking the specifications of the FD-SOI technology offered by the foundry.

BACK-BIAS

With FD-SOI on ultra-thin Buried Oxide (BO_x), the substrate underneath the BO_x is normally tied to V_{dd} or Gnd. This is not disruptive for the design and is handled by substrate ties exactly in the same way as well biasing in classical bulk CMOS technology; only now the contact to the substrate is made through the BO_x.

Then there is the option to have “active” back-bias, to shift the VT or, equivalently, the I_{on}/I_{off} operating point – by shifting the voltage applied under the BO_x. In particular, dynamic back-biasing is an extremely efficient technique to either boost performance or cut leakage according to the workload. It is more efficient and usable than the similar body-bias technique on bulk, due to a very good body factor plus the ability to push significantly further the bias voltage without unacceptable leakage. The bias voltage is applied under the BO_x using the same substrate tie cells as above, placed in the chip layout every so many microns (PDK-dependent), like bulk substrate ties.

MEMORY COMPILERS

For easy porting, the bitcells provided in the FD-SOI PDK should have the same abstract (footprint) as those provided with the bulk CMOS PDK.

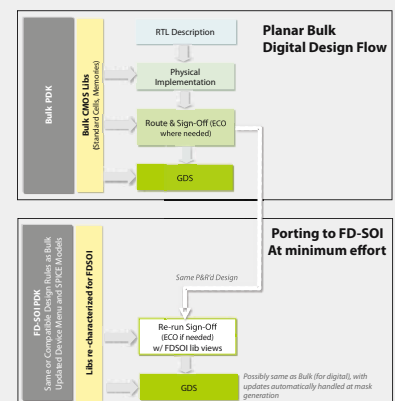
Then existing compilers can be re-used, with updated characterization (timing, power, etc.). For the periphery, options are the same as for standard cells: direct port for fastest time-to-market or re-optimization for ultimate performance.

I/Os AND ANALOG

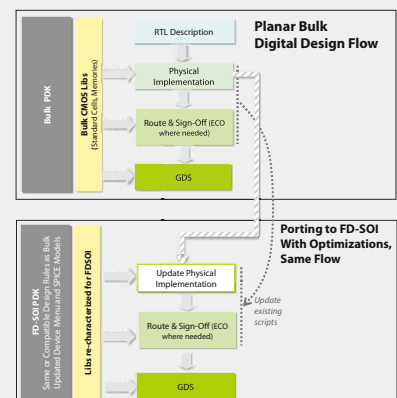
Integration of thick gate-oxide transistors on FD-SOI is not an issue. Non-FET devices will have a counterpart in the FD-SOI device menu. Some of them may actually be provided as Bulk devices, through Bulk-FD-SOI co-integration (by locally etching off the top silicon and BO_x to give access to the

underlying Bulk substrate). In some cases and depending on foundry choices, there might be a few devices used in the original Bulk design that have no direct counterpart in the FD-SOI-compatible device menu: then it would be necessary to adapt the IP design to come up with a solution based on replacement devices. ●

SOC PORTING STRATEGY & DESIGN FLOW



Straight SOC Porting: wherein the least possible effort is required (that is, where the ideal case would be reusing the GDS as is).



Re-optimized SOC implementation: wherein the design team is prepared to invest in a little more specific design to enjoy further benefits of the FD-SOI technology (for example, by introducing dynamic back-bias in a SOC that did not use any).

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Advanced Substrate Industry

What's New. What's Hot. What's Next.

Buzz



> **Freescale** is leveraging its leading-edge 45nm SOI technology for key new products:

- Sampling has begun of the first PSC913x family of "base station-on-chip" QorIQ Converge multimode platform products. These chips, which created a huge buzz when announced in Barcelona last winter at the Mobile World Congress, are at the heart of the Alcatel-Lucent lightRadio™ technology. They simultaneously support multiple air interfaces, providing operators and OEMs "future-proof", highly integrated heterogeneous solutions that help minimize power consumption, cost and design time.
- The new QorIQ™ P2041 quad-core processor for security and other networking equipment delivers up to 10 Gb/s performance and operates at 12W typical power.

> **NXP's** hugely successful SOI-based ABCD technology continues driving key new products:

- Continuing its long line of SOI-based automotive CAN transceivers, NXP announced the next-gen TJA1048 for automotive engine, body control and gateway apps. SOI enables extremely low emission and high immunity against EMI, and protects the bus pins against transients in the automotive environment.



- The new GreenChip SSL4101T is NXP's latest controller IC for Solid State LED lighting power supplies. Its industry-leading performance includes Total Harmonic Distortion (THD) of less than 20 percent, a high Power Factor (PF) of .99, and high efficiency of 94%.



> Built on 45nm SOI CMOS by **IBM** researchers, a new generation of neurosynaptic computing chips is designed to emulate the brain's abilities for perception, action and cognition. The next phase of the project has received \$21 million in new funding from DARPA.

NEW WII U: 45nm SOI



Leveraging its Power Architecture, **IBM** will produce the CPUs for **Nintendo's** hot new Wii U on 45nm SOI. IBM's unique embedded DRAM on SOI (first described in ASN#6) triples the amount of memory on a single chip, feeding the multi-core processor large chunks of data for a smooth and extreme entertainment experience. The Wii U hits store shelves in 2012.

> Leveraging IBM's RF SOI process, fabless **RDA Microelectronics** of Shanghai developed the RDASW91, the world's first single-pole, nine-throw (SP9T) antenna switch with an integrated logic decoder and low pass filters in a single die solution. The target is the fast-growing multiband 3G handset market, wherein SOI offers superior performance and significant cost reduction compared to GaAs alternatives.

> **The Portland Group**, a wholly-owned subsidiary of STMicroelectronics and a leading supplier of compilers for high-performance computing (HPC), has announced its products now include support for AMD's SOI-based "Bulldozer" chips.



> **SiTime's** SOI-based MEMS technology (first described in ASN12) has pushed the company to the forefront of a hot new market:

- With 85% market share and over 75 million of its devices shipped, SiTime is driving the \$5 Billion timing market's transition to 100% silicon-based timing. Targets are telecom, networking, storage and wireless apps.
- The new SiT9121 and SiT9122 oscillators feature 10 PPM stability and only 500 femtoseconds of jitter, a unique combination only available from SiTime.
- The new SiT500x family is the industry's first Voltage Controlled, Temperature Compensated Oscillator (VCTCXO) products with ± 0.5 PPM stability.

> New SOI-based process technology from **TowerJazz** for wireless antenna switches costs substantially less than competing compound solutions, and integrates control functions, low-noise amplifiers and power amplifiers on a single chip. For both high-end smart-phones and lower-end phones, the company says SOI can benefit most of the 1.4 billion handset units sold each year.

THANK YOU!

A special thanks goes to AMD, ARM, EVG, Freescale, IBM, IC Knowledge LLC, IEEE, NXP, STMicroelectronics, the SOI Industry Consortium and Soitec for their help with this issue.

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